# Evaluation of Delays Induced by Foundation Fieldbus H1 Networks

Qingfeng Li, *Member, IEEE*, Drew J. Rankin, *Student Member, IEEE*, and Jin Jiang, *Senior Member, IEEE*

***Abstract*—The delays associated with the use of Foundation Fieldbus (FF) H1 networks within control loops are investigated in this paper. A Smar IF302 device, a Smar FI302 device, a DeltaV distributed control system (DCS), a Honeywell C300 DCS, and a National Instrument (NI) FF H1 workstation are used to implement test loops with the control-in-the-field architecture. Analytical and experimental evaluations are performed with a test loop using hardwired analog channels as a benchmark. Three segments of FF-H1-network-induced delays are identified, their analytical models are developed, and suggestions to potentially reduce the delays are provided. Furthermore, it is found that an unexpected additional delay of one macrocycle may be introduced, probably depending on whether the analog input (AI) block within the IF302 device is executed as scheduled. In conclusion, significant delays could be introduced if the traditional analog channels of a DCS are replaced by an FF H1 network.**

***Index Terms*—Communication systems, delay effects, delay estimation, digital communication, distributed control.**

## NOMENCLATURE

| | |
|---|---|
| $t_{\mathrm{SI}}$ | Control program scan interval. |
| $t_{\mathrm{M}}$ | Foundation Fieldbus (FF) H1 macrocycle. |
| $t_{\mathrm{HW}}$ | Loop-back time of a test loop using hardwired analog channels. |
| $t_{\mathrm{HW1}}$ | First segment of $t_{\mathrm{HW}}$. |
| $t_{\mathrm{HW2}}$ | Second segment of $t_{\mathrm{HW}}$. |
| $\bar{t}_{\mathrm{HW}}$ | Mean of $t_{\mathrm{HW}}$. |
| $\sigma_{\mathrm{HW}}$ | Standard deviation of $t_{\mathrm{HW}}$. |
| $t_{\mathrm{P}}$ | Processing time of a distributed control system (DCS) using analog channels. |
| $t_{\mathrm{PI}}$ | Processing interval of a DCS using analog channels. |
| $t_{\mathrm{CiF}}$ | Loop-back time of test loops using FF H1 networks with the control-in-the-field architecture. |
| $t_{\mathrm{CiF1}}$ | First segment of $t_{\mathrm{CiF}}$. |
| $t_{\mathrm{CiF2}}$ | Second segment of $t_{\mathrm{CiF}}$. |
| $t_{\mathrm{CiF3}}$ | Third segment of $t_{\mathrm{CiF}}$. |
| $p$ | Probability of $t_{\mathrm{CiF2}} = t_{\mathrm{M}}$. |
| $\bar{t}_{\mathrm{CiF}}$ | Mean of $t_{\mathrm{CiF}}$. |
| $t_{\mathrm{SA}}$ | Signal acquisition time of FF H1 devices. |
| $t_{\mathrm{SAI}}$ | Signal acquisition interval of FF H1 devices. |

Manuscript received April 25, 2008; revised October 20, 2008. First published July 24, 2009; current version published September 16, 2009. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada and in part by the University Network of Excellence in Nuclear Engineering. The Associate Editor coordinating the review process for this paper was Dr. Antonios Tsourdos.

The authors are with the Department of Electrical and Computer Engineering, University of Western Ontario, London, ON N6A 5B9, Canada (e-mail: jjiang@eng.uwo.ca).

Digital Object Identifier 10.1109/TIM.2009.2019312

## I. INTRODUCTION

IT HAS long been realized that the use of digital industrial networks within control loops can bring many benefits such as reduced wiring and enhanced communication capabilities [1], but they can also have some consequences such as delays, possible data loss, and quantization errors [2]. Therefore, many studies have been conducted to understand the effects of networks in network-based control systems (NCSs) [3]–[20]. Among these studies, most are devoted to the investigation of network-induced delays, which could have serious impacts on the stability and performance of overall control systems. Consequently, the network-induced delays of almost all major industrial networks have been examined, and various models to describe these delays have been developed. These networks include: 1) Foundation Fieldbus (FF) H1 [3]–[11]; 2) CAN [11]–[14]; 3) Profibus [11], [13]–[17]; 4) Modbus [13]; 5) SERCOS [15]; 6) FIP [15]; and 7) Ethernet [11], [18]–[20].

From a practical point of view, it is reasonable to define network-induced delays as the additional time needed when the analog channels used by DCSs are replaced by digital networks. Given the definition, there will be two kinds of network-induced delays: 1) communication delays and 2) delays associated with filtering, analog-to-digital conversion (ADC), digital-to-analog conversion (DAC), and the execution of function blocks to perform functions such as analog input (AI), analog output (AO), and proportional–integral–derivative (PID) control. In an NCS, most, if not all, of these events occur at field devices. This could result in large delays because the execution speed of the field devices is usually much lower than that of the DCS using analog channels. Therefore, both kinds of delays should be considered. Unfortunately, although the FF H1 network is one of the most widely used networks in process industries, previously published studies on FF-H1-network-induced delays only take into account communication delays [3]–[11].

Most of the previous studies investigate FF-H1-network-induced delays using analytical and/or simulation approaches [6]–[11]; only a few use experimental methods [3]–[5]. Among these experimental studies, that of Pang and Nishitani has measured the time from the data request to the data reception [3]. The time is only a fraction of communication delays. In addition, Hong *et al.* have proposed and implemented a new bandwidth allocation scheme and a new scheduling method for FF H1 networks and experimentally measured communication delays [4], [5].

In this paper, the network-induced delays within control loops are studied from a practical point of view. Commercial

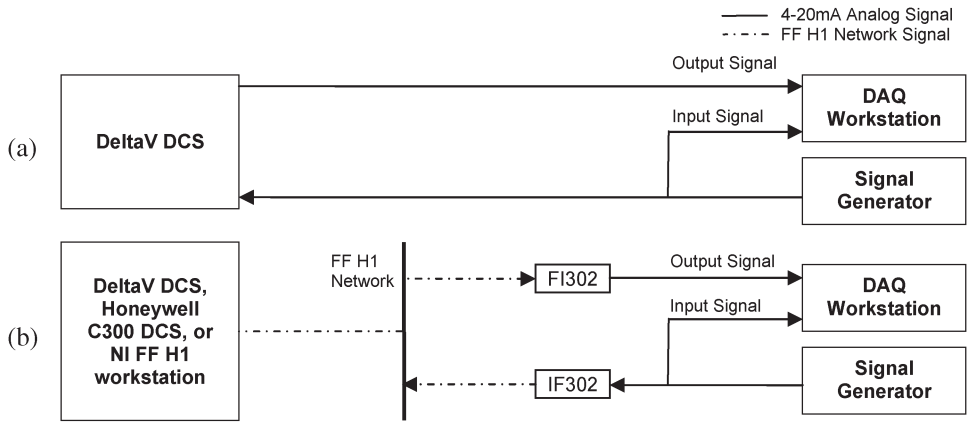



Fig. 1. Test loops using (a) analog channels and (b) an FF H1 network.

FF H1 products and DCSs are used to form FF-H1-network-based test loops. Both analytical and experimental evaluations are performed to investigate the delays introduced to the loops. The segments of the delays are identified, their analytical models are developed, and suggestions to potentially reduce them are provided.

The results in this paper are valuable for practical control system applications. Control engineers can use the analytical models to estimate the delays induced by FF H1 networks and then assess their impacts on the control system stability and performance. In addition, they can also follow the suggestions to reduce the network-induced delays.

This paper is organized as follows. The problem statement and the scope of investigation are given in Section II. Section III introduces the experimental setups and approaches. Section IV analyzes the test loops using analog channels and FF H1 networks, respectively. Experimental evaluations are covered in Section V. Conclusions and recommendations are presented in Section VI.

## II. Problem Statement and Scope of Investigation

This paper addresses the delays introduced when FF H1 networks are used to replace traditional analog channels. Both analytical and experimental evaluations are carried out with a test loop using analog channels as the benchmark. However, the effects of such delays on the control system stability and performance are not investigated herein.

The investigated loops are single loops consisting of a Smar IF302 device, a Smar FI302 device, and an FF H1 device serving as a link active scheduler (LAS) that schedules and manages activities on the network. The IF302 device converts industrial standard 4–20-mA analog signals to FF H1 signals; the FI302 device converts FF H1 signals back to 4–20-mA analog signals. A network-based control loop will be formed when the IF302 device is connected to a sensor with 4–20-mA output and the FI302 device is connected to an actuator that accepts 4–20-mA input.

In the analytical evaluations, the loop-back time is divided into several segments, and their models are developed. In the experimental evaluations, tests are performed with the IF302 device and the FI302 device connected to a DeltaV DCS, a Honeywell C300 DCS, and a National Instrument (NI) FF H1 workstation, respectively. All the three have their own FF H1 cards that can serve as the LAS for the network.

FF-H1-network-induced delays could be affected by the control program scan interval, the FF H1 macrocycle, and the control architecture. The scan interval, which is denoted by $t_{\mathrm{SI}}$, specifies how often the DCS controller executes the control programs. The time $t_{\mathrm{SI}}$ is referred to as the scan rate by Emerson Process Management (the DeltaV DCS vendor). The FF H1 macrocycle, which is denoted by $t_{\mathrm{M}}$, specifies how often process data are transmitted over the network and function blocks are executed within the field devices [21].

The control architecture can be either control in the field or hybrid. If all function blocks are executed within the field devices, the control architecture is known as control in the field; if some function blocks are executed within the field devices but others are executed within the DCS controller, it is called hybrid. The control-in-the-field architecture can reduce the network load; thus, a shorter macrocycle can be implemented, resulting in reduced network-induced delays; the hybrid architecture allows the implementation of more advanced control algorithms but requires a longer macrocycle. When the control-in-the-field architecture is used, the results of loop-back tests are not influenced by $t_{\mathrm{SI}}$ because no communication between the field devices and the DCS controller is required. In this paper, only the control-in-the-field architecture is evaluated as it is commonly recommended in practice [21].

## III. Experimental Setups and Approaches

The conceptual diagrams of the experimental setups are shown in Fig. 1. In both cases, no control function block is implemented; only one AI block and one AO block are used, and they are directly connected together. Nevertheless, the signal paths of the chosen test loops resemble those of most practical control loops.

In Fig. 1, all the signals are transmitted through twisted-pair cables. The IF302 device, the FI302 device, and the FF H1 card are wired to a Relcom FF H1 power hub. The cable connecting the FF H1 card to the hub is the longest among all the cables. It has a length of 7.5 m and is much shorter than the FF H1 cable length limit of 1900 m [1].

During tests, a low-frequency (0.125–0.5-Hz) square-wave current signal between 10 and 14 mA is generated by the signal

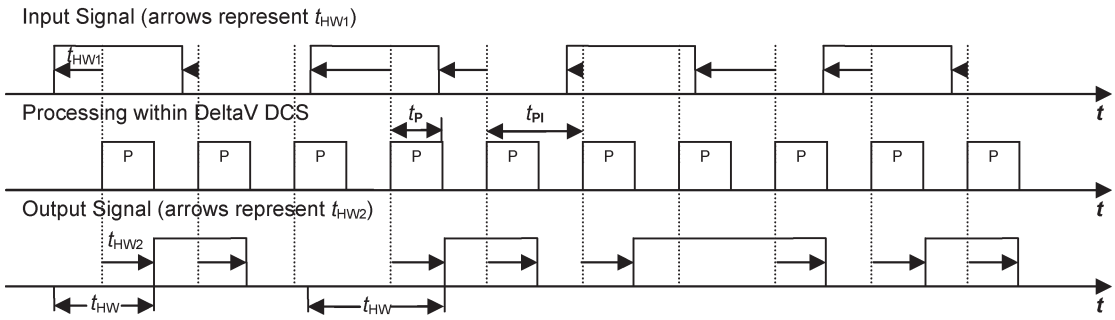



Fig. 2. Illustrative timing diagram of a test loop using analog channels.

generator and injected into the loop. Both the input signal and the return signal, which is referred to as output signal, are captured by the data acquisition (DAQ) workstation at a sampling rate of 100 Hz. The loop-back time is then determined by comparing the two signals.

Since it is critical to ensure the precise timing of the test signals, an NI PCI-6071E DAQ card with direct memory access (DMA) mode is used. Under DMA mode, data are directly exchanged between the DAQ card and the workstation memory. This assures that signal generation and acquisition are independent of the central processing unit (CPU) of the workstation. In addition, the accuracy of the timing is verified with a Tektronix TDS210 oscilloscope.

## IV. Analytical Evaluations of Network-Induced Delays

### A. Delays Within a Test Loop Using Analog Channels

The illustrative timing diagram of the test loop shown in Fig. 1(a) is presented in Fig. 2. In the figure, P stands for the processing within the DCS. During a loop-back process, the following sequence of events will occur: 1) the ADC at the AI card acquires the input signal from the signal generator; 2) the DCS controller reads data from the AI card through one I/O scan; 3) the controller executes the program consisting of only one AI block and one AO block; 4) the controller sends data to the AO card through another I/O scan; and 5) the AO card updates its output. The control program scan interval is at least twice the I/O scan interval [22].

It is assumed that both the processing time of the DCS (denoted by $t_{\rm P}$) and the processing interval (denoted by $t_{\rm PI}$) are deterministic, as shown in Fig. 2. Under this assumption, $t_{\rm PI}$ will be equal to $t_{\rm SI}$ as the processing is performed once every scan interval.

The loop-back time $t_{\rm HW}$ can be divided into two segments, as shown in Fig. 2. Since the signal generator is independent of the DCS, the probability for a step change to occur anywhere within a scan interval will be the same. Therefore, it is assumed that $t_{\rm HW1}$ follows a uniform distribution between 0 and $t_{\rm SI}$. The duration of $t_{\rm HW2}$ is equal to $t_{\rm P}$, and it is not affected by $t_{\rm SI}$. Under these assumptions, the mean and the standard deviation of $t_{\rm HW}$ can be shown as follows:

$$\bar{t}_{\rm HW} = 0.5t_{\rm SI} + t_{\rm P} \tag{1}$$

$$\sigma_{\rm HW} = t_{\rm SI}/\sqrt{12} \tag{2}$$

where $\bar{t}_{\rm HW}$ is the mean, and $\sigma_{\rm HW}$ is the standard deviation of $t_{\rm HW}$. The largest value of $t_{\rm HW}$ is $t_{\rm SI} + t_{\rm P}$, and the smallest is $t_{\rm P}$.

### B. Delays Within a Test Loop Using an FF H1 Network

The illustrative timing diagram of the test loop shown in Fig. 1(b) is presented in Fig. 3. In the figure, SA stands for the signal acquisition of the IF302 device, AI stands for the execution of the AI block within the IF302 device, C stands for the communication through the network, and AO stands for the execution of the AO block within the FI302 device. The loop-back time $t_{\rm CiF}$ can be divided into three segments, as shown in the figure.

The segment $t_{\rm CiF1}$ is the time between the step change of the input signal and the beginning of the execution of the AI block within the IF302 device. It is assumed that $t_{\rm CiF1}$ follows a uniform distribution between 0 and $t_{\rm M}$ as the signal generator is independent of the IF302 device.

The segment $t_{\rm CiF2}$ represents one or more macrocycles that may be needed because it is possible that a complete signal acquisition does not exist within $t_{\rm CiF1}$. Although the IF302 device periodically acquires the input signal, the acquisition is not synchronized with the macrocycle. The time needed to complete one acquisition, which is denoted by $t_{\rm SA}$, is 100 ms; the acquisition interval, which is denoted by $t_{\rm SAI}$, is 300 ms as the device has three channels. The duration of $t_{\rm SAI}$ remains the same even if only one channel is in use [23].

The segment $t_{\rm CiF3}$ is the time that elapses before the completion of the initial 10% rise/fall of the output signal. During $t_{\rm CiF3}$, the following sequence of events will occur: 1) the execution of the AI block within the IF302 device; 2) the communication between the IF302 device and the FI302 device; 3) the execution of the AO block within the FI302 device; and 4) the update of the analog output of the FI302 device. In fact, within events 1) and 3), the transducer blocks associated with the AI block and the AO block are also executed. The transducer blocks perform device-specific functions so that standard function blocks can be used [24].

Among the four events, event 1) is scheduled to take 45 ms, and event 3) is scheduled to take 50 ms. The time scheduled for event 2) is between 17 and 39 ms in the experimental tests. The analog output of the FI302 device is generated by consecutively sending a pulse-width modulation signal through two first-order low-pass filters whose cut frequencies are 1.5915 Hz [23]. As

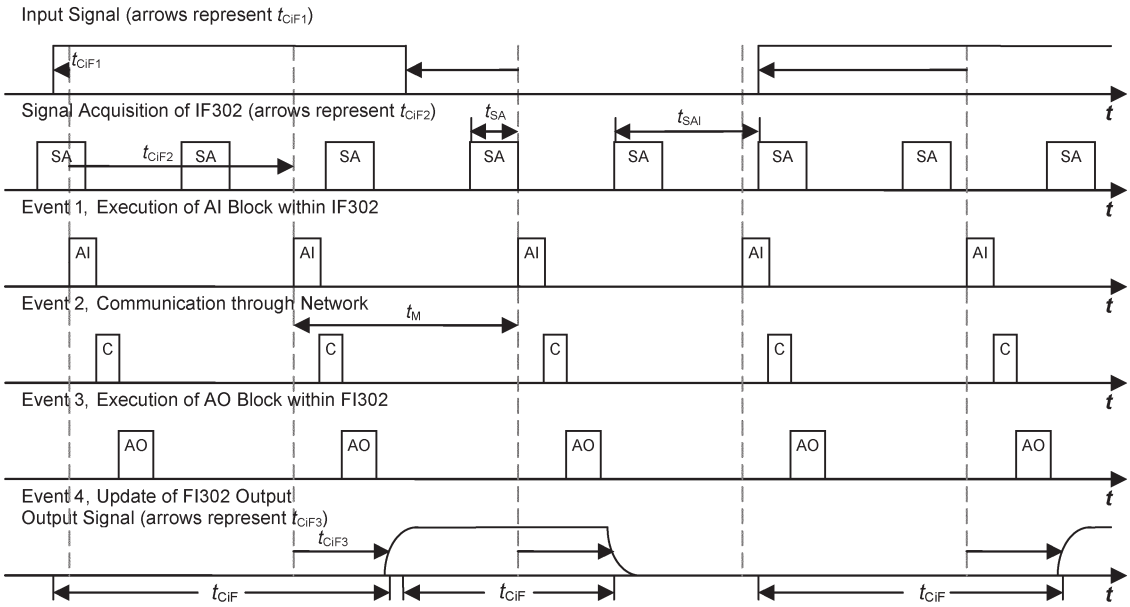



Fig. 3. Illustrative timing diagram of a test loop using an FF H1 network.

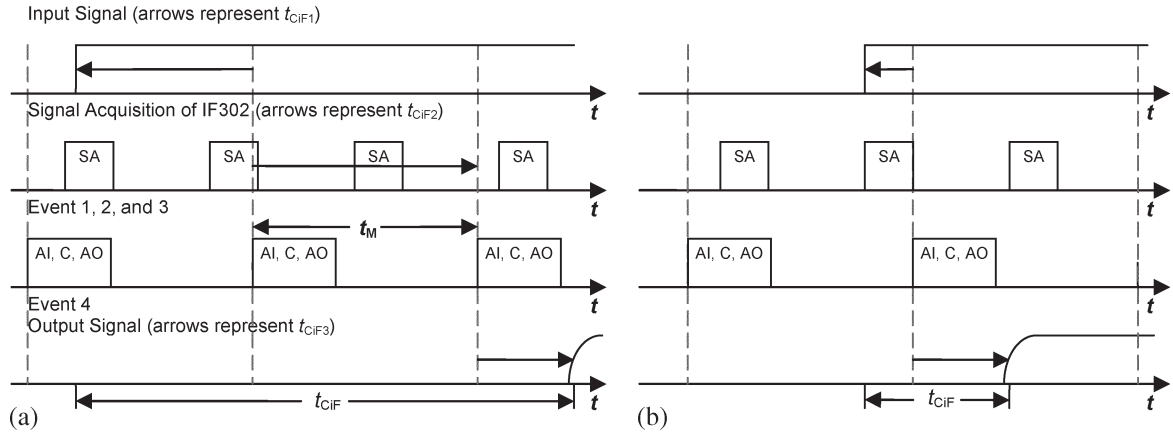



Fig. 4. Illustrative timing diagram of loop-back using an FF H1 network. (a) Worst-case scenario. (b) Best-case scenario.

a result, the time taken by event 4) is almost equal to the time needed for the FI302 output signal to complete its initial 10% rise/fall. Depending on the FF H1 schedule adopted, there may be some idle time between the execution of the AI block, the communication, and the execution of the AO block.

Since the signal acquisition of the IF302 device is not synchronized with the macrocycle, it is reasonable to assume that the time between the beginning of the execution of the AI block and the beginning of the preceding acquisition of the input signal follows a uniform distribution between $t_{\rm SA}$ and $t_{\rm SA}+t_{\rm SAI}$. In addition, it is also assumed that $t_{\rm M}\geq t_{\rm SA}+t_{\rm SAI}$ to ensure that $t_{\rm CiF2}\leq t_{\rm M}$ is true. Under these assumptions, it can be shown that

$$p=\begin{cases}1, & t_{\rm CiF1}<t_{\rm SA}\\ \dfrac{t_{\rm SA}+t_{\rm SAI}-t_{\rm CiF1}}{t_{\rm SAI}}, & t_{\rm SA}\leq t_{\rm CiF1}<t_{\rm SA}+t_{\rm SAI}\\ 0, & t_{\rm CiF1}\geq t_{\rm SA}+t_{\rm SAI}\end{cases} \tag{3}$$

where $p$ is the probability of $t_{\rm CiF2}=t_{\rm M}$. Consequently

$$\bar{t}_{\rm CiF}=0.5t_{\rm M}+t_{\rm SA}+0.5t_{\rm SAI}+t_{\rm CiF3} \tag{4}$$

where $\bar{t}_{\rm CiF}$ is the mean of $t_{\rm CiF}$. The largest value of $t_{\rm CiF}$ is $t_{\rm M}+t_{\rm SA}+t_{\rm SAI}+t_{\rm CiF3}$, and the smallest is $t_{\rm SA}+t_{\rm CiF3}$. The two values correspond to the worst-case and the best-case scenarios, as shown in Fig. 4.

When the control-in-the-field architecture is used, control algorithms will reside within either the IF302 device or the FI302 device. In either case, both $t_{\rm CiF1}$ and $t_{\rm CiF2}$ represent sensor-to-controller delays. Therefore, sensor-to-controller delays account for most of the FF-H1-network-induced delays.

## V. Experimental Evaluations of Network-Induced Delays

### A. Tests With a Loop Using Analog Channels

The tests with the loop shown in Fig. 1(a) are performed with $t_{\rm SI}$ set to 100, 200, and 500 ms, respectively. The frequency of the input signal is 0.5 Hz when $t_{\rm SI}$ is 100 or 200 ms and 0.25 Hz when $t_{\rm SI}$ is 500 ms.

The input signal shown in Fig. 2 is not synchronized with the scan interval. As a result, it is difficult to ensure that $t_{\rm HW1}$ adequately covers the whole range of its distribution with a

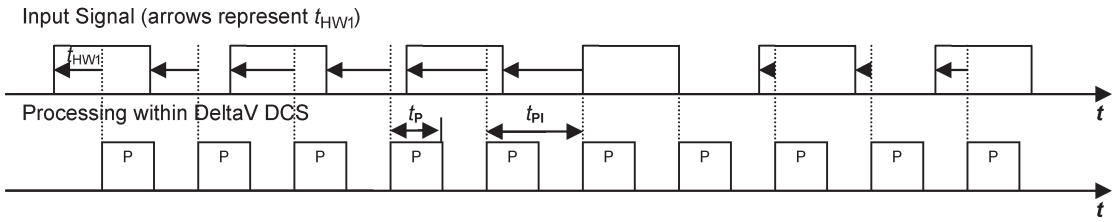



Fig. 5. Illustrative timing diagram with a time-shifted input signal.

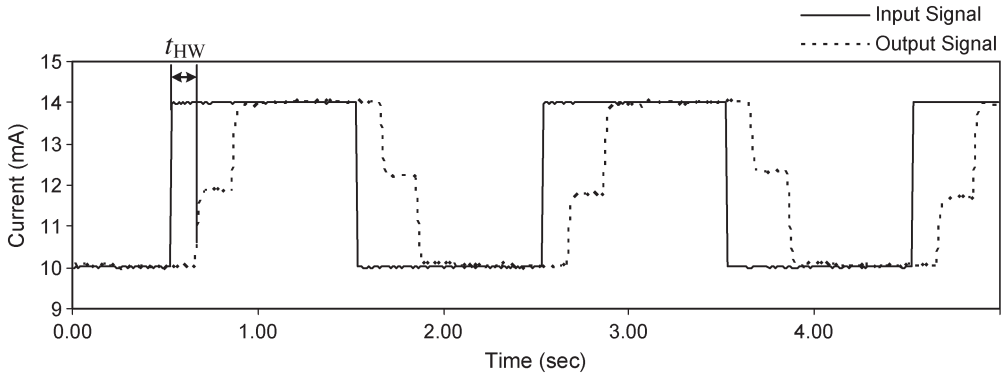



Fig. 6. Sample test results with a test loop using analog channels.

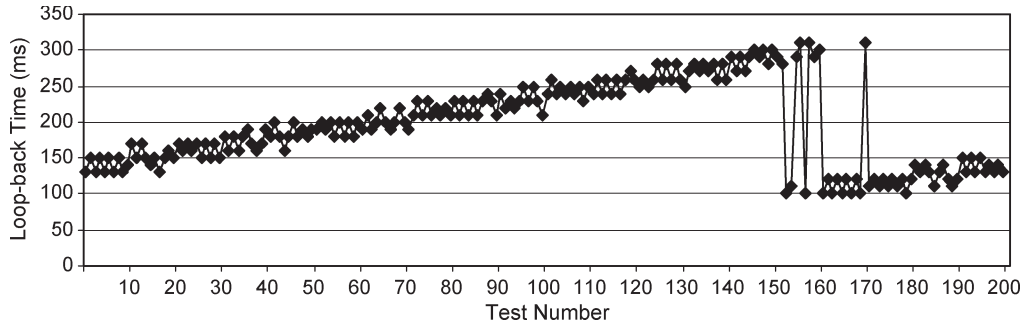



Fig. 7. Measured $t_{\mathrm{HW}}$ with a $t_{\mathrm{SI}}$ of 200 ms.

certain amount of loop-back tests. To address this issue, during the tests, the input signal is synchronized with the scan interval but time shifted every five cycles. The time-shift step is 10 ms for a $t_{\mathrm{SI}}$ of 100 or 200 ms and 20 ms for a $t_{\mathrm{SI}}$ of 500 ms. The mechanism of the time shifting is demonstrated in Fig. 5.

Sample test results with a $t_{\mathrm{SI}}$ of 200 ms are presented in Fig. 6. Although the input signal is perfectly square, the output signal could contain some glitches, i.e., it may take several steps to complete a rise/fall. These glitches are due to both the low sampling rate and the dynamics introduced by the low-pass filter within the DeltaV AI card, as square signals contain high-frequency components. To be more specific, when the input signal passes through the low-pass filter, it will no longer be a square wave. If a sampling is performed during a rise/fall of the input signal, a value somewhere between 10 and 14 mA will be sent to the controller, and a glitch will appear when the output of the AO card is updated. Each glitch lasts about 200 ms, as the sampling is performed only once every 200 ms. The duration of $t_{\mathrm{HW}}$ is determined by comparing the input and output signals, as shown in the figure.

The measured $t_{\mathrm{HW}}$ with a $t_{\mathrm{SI}}$ of 200 ms is shown in Fig. 7. In the figure, each point corresponds to one loop-back test. Since the input signal is time shifted every five cycles, ten loop-back tests are performed at each time shift. Tests 1–10 are performed at the first time shift, test 11–20 are performed at the second time shift, and so on. With the change of $t_{\mathrm{HW1}}$ due to the time shifting, the measured $t_{\mathrm{HW}}$ differs at different time shifts. The variance of $t_{\mathrm{HW}}$ is much larger at the sixteenth and seventeenth time shifts. At these two shifts, if a complete signal acquisition exists between the step change of the input signal and the execution of the AI block, $t_{\mathrm{HW}}$ will be around 100 ms; else, it will be around 300 ms, i.e., 100 ms plus one scan interval.

TABLE I
COMPARISONS BETWEEN MEASURED AND ESTIMATED $t_{\mathrm{HW}}$

| $t_{\mathrm{SI}}$ (ms) | Measured or Estimated | Mean (ms) | Std. Dev. (ms) | Min (ms) | Median (ms) | Max (ms) |
|---|---|---|---|---|---|---|
| 100 | Measured | 149 | 31 | 80 | 150 | 220 |
| | Estimated | 149 | 29 | 99 | N/A | 199 |
| 200 | Measured | 197 | 58 | 100 | 200 | 310 |
| | Estimated | 199 | 58 | 99 | N/A | 299 |
| 500 | Measured | 351 | 145 | 100 | 360 | 620 |
| | Estimated | 349 | 144 | 99 | N/A | 599 |

The measured and the estimated $t_{\mathrm{HW}}$ relative to different $t_{\mathrm{SI}}$ are presented in Table I. The duration of $t_{\mathrm{P}}$ is determined to

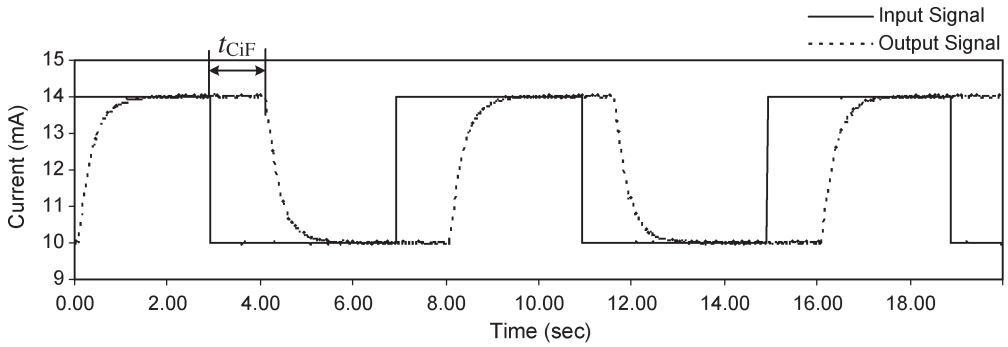



Fig. 8. Sample test results with a test loop using an FF H1 network.

TABLE II
FF H1 SCHEDULE USED IN EACH TEST CONFIGURATION

| Test Configuration | Time Offset from the Beginning of Macrocycle | | |
|---|---|---|---|
| | AI Block (ms) | Communication (ms) | AO Block (ms) |
| DeltaV Default | 0 | 45 | 75 |
| Honeywell Default | 0 | 200 | 217 |
| NI Default | 0 | 43 | 82 |
| NI Modified | 0 | 200 | 239 |

be 99 ms using the test results with a $t_{\mathrm{SI}}$ of 100 ms. Table I demonstrates that the test results match well with the estimates from (1) and (2).

### *B. Tests With a Loop Using an FF H1 Network*

During the tests with the loop shown in Fig. 1(b), the frequency of the test signal is set to be 0.125 Hz. The input signal is synchronized with the macrocycle but time shifted every five cycles. The time-shift step is 50 ms.

Sample test results with a $t_{\mathrm{M}}$ of 500 ms while using the DeltaV DCS are shown in Fig. 8. The first-order dynamics of the output signal are due to the low-pass filters within the FI302 device. The measured rise/fall time of the output signal is around 640 ms. The duration of $t_{\mathrm{CiF}}$ is determined by comparing the input and output signals, as shown in the figure.

Tests are performed with the IF302 device and the FI302 device connected to the DeltaV DCS, the Honeywell C300 DCS, and the NI FF H1 workstation, respectively. Among the three, only the NI FF H1 workstation allows the FF H1 schedule to be modified. The schedule adopted for each test configuration is presented in Table II. The idle time between the execution of the AI block and the communication is 155 ms with the configuration of Honeywell Default or NI Modified.

The measured $t_{\mathrm{CiF}}$ with a $t_{\mathrm{M}}$ of 500 ms is presented in Fig. 9 and Table III. In the figure, each point corresponds to one loop-back test, and ten loop-back tests are performed at each time shift. With the change of $t_{\mathrm{CiF1}}$ due to the time shifting, the measured $t_{\mathrm{CiF}}$ differs at different time shifts. The variance of $t_{\mathrm{CiF}}$ could be large even at the same time shift. That is partially because $t_{\mathrm{CiF2}}$ may be equal to 0 or $t_{\mathrm{M}}$, depending on whether a complete signal acquisition exists within $t_{\mathrm{CiF1}}$.

Using the analytical evaluation results, the estimated $t_{\mathrm{CiF}}$ with a $t_{\mathrm{M}}$ of 500 ms is presented in Tables III and IV. Among the estimated $t_{\mathrm{CiF}}$, the time for the output signal to complete the initial 10% rise/fall is estimated to be 30 ms, with the measured rise/fall time using the formula describing first-order step responses.

The measured $t_{\mathrm{CiF}}$ with the configurations of Honeywell Default and NI Modified is slightly shorter than the estimated one, as shown in Table III. The small differences could be due to the nondeterminism of $t_{\mathrm{SA}}$ and $t_{\mathrm{SAI}}$.

Comparatively, the measured $t_{\mathrm{CiF}}$ with the configurations of DeltaV Default and NI Default is significantly longer than the estimated one, as shown in Table III. In fact, the test results indicate an unexpected additional delay of one macrocycle may be included in $t_{\mathrm{CiF}}$. In Fig. 9(a) and (c), the range of the measured $t_{\mathrm{CiF}}$ is about 1000 ms at some time shifts. The 1000 ms is the total of one macrocycle corresponding to $t_{\mathrm{CiF2}}$ plus the additional delay of one macrocycle. In addition, the difference between the largest values of the measured and the estimated $t_{\mathrm{CiF}}$ with the configuration of DeltaV Default is 365 ms, and the difference with the configuration of NI Default is 338 ms. Both values are close to one macrocycle.

The measured $t_{\mathrm{CiF}}$ with a $t_{\mathrm{M}}$ of 1000 ms and the configuration of DeltaV Default is shown in Fig. 10. In the figure, the range of the measured $t_{\mathrm{CiF}}$ is about 2000 ms at some time shifts. In addition, the difference between the largest values of the measured and the estimated $t_{\mathrm{CiF}}$ is 865 ms, which is also close to one macrocycle. These observations confirm the existence of the additional delay of one macrocycle.

The existence of the additional delay is dependent on the FF H1 schedule. When the configuration of DeltaV Default is used, only 45 ms is assigned for the execution of the AI block. As a result, additional delays may be introduced, probably because the execution of the AI block either: 1) cannot complete within the assigned 45-ms period or 2) does not start at the scheduled time. When the configuration of Honeywell Default is used, 200 ms is assigned for the execution of the AI block; consequently, the additional delay disappears, as shown in Fig. 9(b). The fact is further confirmed by the test results with the configurations of NI Default and NI Modified. Although the insertion of a 155-ms time slot between the execution of the AI block and the communication significantly increases $t_{\mathrm{CiF3}}$, it eliminates the additional delay, as shown in Fig. 9(d).

A comparison between $t_{\mathrm{HW}}$ and $t_{\mathrm{CiF}}$ indicates that significant delays could be introduced if traditional analog channels of a DCS are replaced by an FF H1 network. The distributions

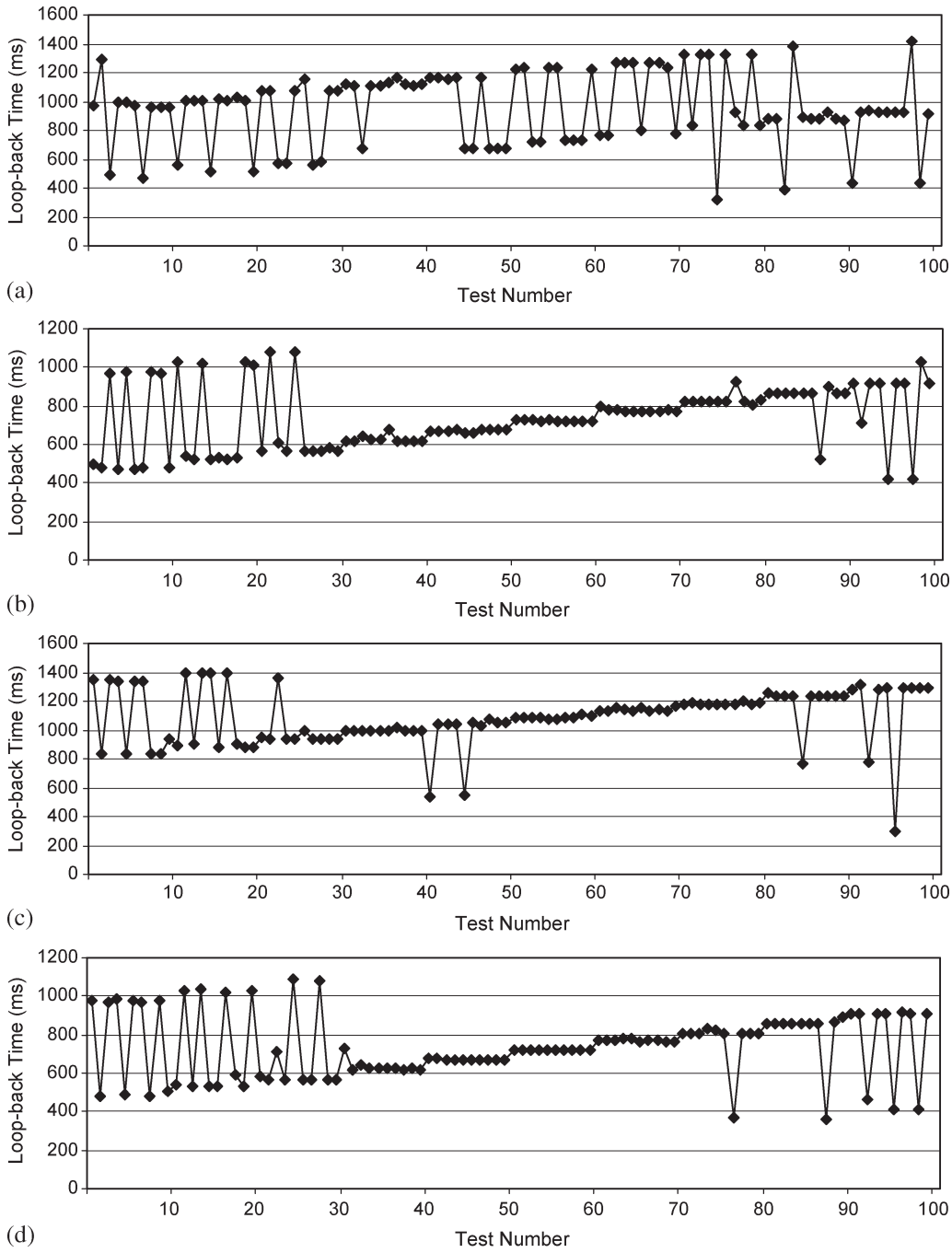



Fig. 9. Measured $t_{\mathrm{CiF}}$ with a $t_{\mathrm{M}}$ of 500 ms and the configuration of (a) DeltaV Default, (b) Honeywell Default, (c) NI Default, and (d) NI Modified.

TABLE III
COMPARISONS BETWEEN MEASURED AND ESTIMATED $t_{\mathrm{CiF}}$

| Test Configuration | Measured or Estimated | Mean (ms) | Std. Dev. (ms) | Min (ms) | Median (ms) | Max (ms) |
|---|---|---|---|---|---|---|
| DeltaV Default | Measured | 950 | 258 | 320 | 965 | 1420 |
| | Estimated | 655 | N/A | 255 | N/A | 1055 |
| Honeywell Default | Measured | 736 | 163 | 420 | 725 | 1080 |
| | Estimated | 797 | N/A | 397 | N/A | 1197 |
| NI Default | Measured | 1087 | 191 | 300 | 1090 | 1400 |
| | Estimated | 662 | N/A | 262 | N/A | 1062 |
| NI Modified | Measured | 736 | 167 | 360 | 720 | 1090 |
| | Estimated | 819 | N/A | 419 | N/A | 1219 |

TABLE IV
SEGMENTS OF ESTIMATED $t_{\mathrm{CiF}}$

| Test Configuration | $t_{\mathrm{CiF1}}$ (ms) | $t_{\mathrm{CiF2}}$ (ms) | $t_{\mathrm{CiF3}}$ (ms) |
|---|---|---|---|
| DeltaV Default | 0 to 500 | 0 or 500 | 155 |
| Honeywell Default | | | 297 |
| NI Default | | | 162 |
| NI Modified | | | 319 |

of $t_{\mathrm{HW1}}$ and $t_{\mathrm{CiF1}}$ are equal if the $t_{\mathrm{SI}}$ of the loop using analog channels is equal to the $t_{\mathrm{M}}$ of the loop using FF H1 networks. However, for the same application the $t_{\mathrm{SI}}$ of the loop using

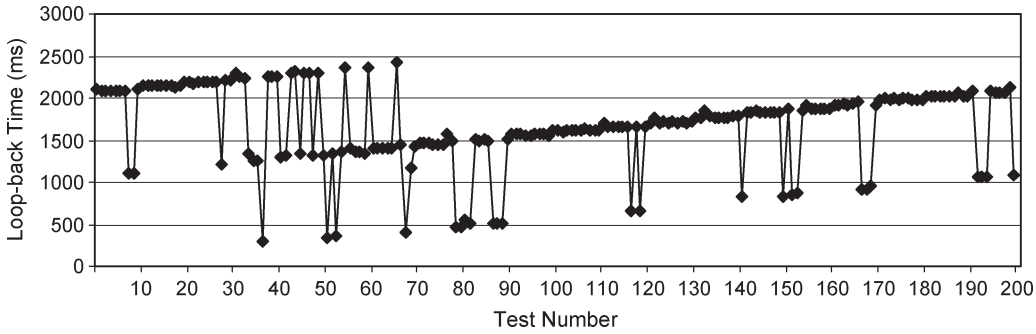



Fig. 10. Measured $t_{\mathrm{CiF}}$ with a $t_{\mathrm{M}}$ of 1000 ms and the configuration of DeltaV Default.

analog channels can be much shorter than the $t_{\mathrm{M}}$ of the loop using FF H1 networks. Meanwhile, $t_{\mathrm{HW2}}$ can be much shorter than the total of $t_{\mathrm{CiF2}}$ and $t_{\mathrm{CiF3}}$ because in the loop using analog channels, the execution speed of controllers, ADC, and DAC are higher and the signal acquisition is performed at a higher rate. Moreover, $t_{\mathrm{CiF}}$ may include an additional delay of one macrocycle.

The significant network-induced delays are evident with a comparison between Tables I and III. For example, the mean of the measured $t_{\mathrm{HW}}$ with a $t_{\mathrm{SI}}$ of 500 ms is 351 ms; the mean of the measured $t_{\mathrm{CiF}}$ with a $t_{\mathrm{M}}$ of 500 ms is between 736 and 1087 ms.

Even though the results reported in this paper are for single-loop cases, when one FF H1 network is used to implement two or more loops, only the communications over the network have to be executed in series. The function blocks of the multiple loops are often simultaneously executed. Therefore, the obtained results are still applicable in principle. However, the network-induced delays could become less significant as all the function blocks have to be executed in the DCS controller when analog channels are used.

## VI. Conclusion and Recommendations

This paper has indicated that FF-H1-network-induced delays could be significant and has suggested several ways to reduce them. First, the macrocycle should be chosen as short as possible to minimize the first segment of the loop-back time. Second, the signal acquisition time and acquisition interval should be reduced, and the acquisition should be synchronized with the macrocycle to reduce the second segment of the loop-back time. Third, the idle time between the execution of the AI block and the communication, as well as that between the communication and the execution of the AO block, should be eliminated so that the third segment of the loop-back time can be minimized as well.

The experimental tests have also shown that FF H1 networks may introduce an unexpected additional delay of one macrocycle. Consequently, product vendors are recommended to further investigate this problem to eliminate the additional delay and the associated jitters. End users are also recommended to test FF H1 devices with the methodology proposed herein to detect the existence of the additional delay and assess its impacts before installing the devices in industrial applications. Furthermore, Fieldbus Foundation may want to carry out similar tests during the FF H1 product certification process.

## Acknowledgment

The authors would like to thank the technical support staff of Smar, Emerson Process Management, Lakeside Process Controls, and Honeywell for their help in setting up experimental systems and providing valuable information regarding their respective products. The authors would also like to thank the three anonymous reviewers whose constructive comments helped to greatly improve the quality of this paper.

## References

[1] Fieldbus Foundation, *Foundation Fieldbus Technical Overview*, 2003. [Online]. Available: http://www.fieldbus.org/images/stories/technology/developmentresources/development_resources/documents/techoverview.pdf

[2] J. Hespanha, P. Naghshtabrizi, and Y. Xu, "A survey of recent results in networked control systems," *Proc. IEEE*, vol. 95, no. 1, pp. 138–162, Jan. 2007.

[3] Y. Pang and H. Nishitani, "Analysis of control interval for foundation fieldbus-based control systems," *ISA Trans.*, vol. 45, no. 3, pp. 447–458, Jul. 2006.

[4] S. H. Hong and I. H. Choi, "Experimental evaluation of a bandwidth allocation scheme for foundation fieldbus," *IEEE Trans. Instrum. Meas.*, vol. 52, no. 6, pp. 1787–1791, Dec. 2003.

[5] S. H. Hong and S. M. Song, "Transmission of a scheduled message using a foundation fieldbus protocol," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 2, pp. 268–275, Feb. 2008.

[6] S. H. Hong and S. J. Ko, "A simulation study on the performance analysis of the data link layer of IEC/ISA fieldbus," *Simulation*, vol. 76, no. 2, pp. 109–118, Feb. 2001.

[7] Z. Wang, X. Shen, J. Chen, Y. Song, T. Wang, and Y. Sun, "Real-time performance evaluation of urgent a periodic messages in FF communication and its improvement," *Comput. Stand. Interfaces*, vol. 27, no. 2, pp. 105–115, Jan. 2005.

[8] L. Durante and A. Valenzano, "On the performance of the IEC 61158 fieldbus," *Comput. Stand. Interfaces*, vol. 21, no. 3, pp. 241–250, Aug. 1999.

[9] S. Vitturi, "Some features of two fieldbuses of the IEC 61158 standard," *Comput. Stand. Interfaces*, vol. 22, no. 3, pp. 203–215, Aug. 2000.

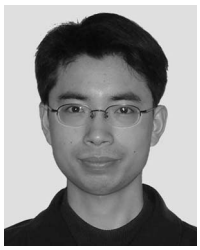
[10] S. Cavalieri, A. Di Stefano, and O. Mirabella, "Optimisation of acyclic bandwidth allocation exploiting the priority mechanism in the fieldbus data link layer," *IEEE Trans. Ind. Electron.*, vol. 40, no. 3, pp. 297–306, Jun. 1993.

[11] Y. Zhou, H. Yu, and T. Wang, "Performance analysis and evaluation of control networks," *Chin. J. Sci. Instrum.*, vol. 27, pp. 492–496, May 2006.

[12] J. Gamiz, J. Samitier, J. M. Fuertes, and O. Rubies, "Practical evaluation of messages latencies in CAN," in *Proc. IEEE Conf. Emerging Technol. Factory Autom.*, 2003, pp. 185–192.

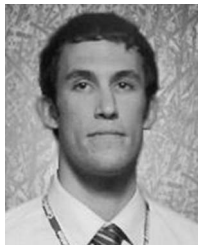
[13] M. D. R. Benito, J. M. Fuertes, E. Kahoraho, and N. P. Arzoz, "Performance evaluation of four fieldbuses," in *Proc. 7th IEEE Int. Conf. Emerging Technol. Factory Autom.*, 1999, pp. 881–890.

[14] M. M. D. Santos, M. R. Stemmer, and F. Vasques, "Evaluation of the timing properties of two control networks: CAN and PROFIBUS," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2003, pp. 874–879.
[15] G. Cena, L. Durante, and A. Valenzano, "Standard field bus networks for industrial applications," *Comput. Stand. Interfaces*, vol. 17, no. 2, pp. 155–167, Jan. 1995.
[16] S. H. Hong, "Experimental performance evaluation of Profibus-FMS," *IEEE Robot. Autom. Mag.*, vol. 7, no. 4, pp. 64–72, Dec. 2000.
[17] S. H. Hong and K. A. Kim, "Implementation and performance evaluation of Profibus in the automation systems," in *Proc. IEEE Int. Workshop Factory Commun. Syst.*, 1997, pp. 187–192.
[18] P. Ferrari, A. Flammini, and S. Vitturi, "Performance analysis of PROFINET networks," *Comput. Stand. Interfaces*, vol. 28, no. 4, pp. 369–385, Apr. 2006.
[19] X. Hao and L. Wu, "Performance evaluation of industrial Ethernet and its modeling," in *Proc. Int. Conf. Inf. Acquisition*, 2004, pp. 527–531.
[20] K. C. Lee, S. Lee, and M. H. Lee, "Worst case communication delay of real-time industrial switched Ethernet with multiple levels," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1669–1676, Oct. 2006.
[21] Emerson Process Management, *Answers to Questions About Implementing Fieldbus in DeltaV Systems*, Mar. 2007. [Online]. Available: http://www.easydeltav.com/pd/WP_Ff_FAQ.pdf
[22] L. Toledo, Emerson Process Management, private communications, Jan. 2008.
[23] M. V. B. Tavares, Smar, private communications, Oct. 2007 and Jul. 2008.
[24] Smar, *Function Blocks Instruction Manual*, Mar. 2005. [Online]. Available: http://www.smar.com/PDFs/Manuals/FBLOC-FFME.PDF



**Qingfeng Li** (M'07) received the Ph.D. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2005.

He is currently a Research Engineer with the Department of Electrical and Computer Engineering, University of Western Ontario, London, ON, Canada. His research interests include distributed control systems, fieldbus technology, and smart devices.



**Drew J. Rankin** (S'04) was born in Windsor, ON, Canada, in 1983. He received the B.App.Sc. (Co-op) (Hons.) degree in electrical engineering from the University of Windsor, Windsor, in 2006 and the M.Eng.Sc. (Thesis) degree in electrical engineering from the University of Western Ontario, London, ON, in 2009. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, University of Western Ontario.

He is currently a member of the Control, Instrumentation and Electrical System Research Group, University of Western Ontario. His research interests include fault-tolerant, predictive, safety critical control, and shutdown systems relating to nuclear power plant systems, hardware-in-the-loop simulation, enhanced control strategies, and advanced digital controller hardware.

Mr. Rankin held the Chair position at the University of Windsor IEEE Student Branch in 2004.

**Jin Jiang** (S'85–M'87–SM'94) received the Ph.D. degree from the University of New Brunswick, Fredericton, NB, Canada, in 1989.

He is currently a Professor with the Department of Electrical and Computer Engineering, University of Western Ontario, London, ON, Canada, and is also the Natural Sciences and Engineering Research Council of Canada/University Network of Excellence in Nuclear Engineering Senior Industrial Research Chair in Control, Instrumentation, and Electrical Systems in Nuclear Power Plants. His research interests include fault-tolerant control systems, theory and application of instrumentation and control systems in nuclear power plants, and distributed power generation involving fuel cells and other renewal energy sources.